REMARKS

Claims 1-25 are pending, where claims 1-15 and 21-22 are withdrawn, and claims 23-25 are new. Claims 16-20 were rejected as being anticipated by USP 6,792,374, hereinafter referred to as "Corr". Applicants traverse the rejection.

First, Applicants request reconsideration of the restriction requirement under 35 CFR 1.111. Applicants request at least the restriction requirement be withdrawn for claims 1-15 on the grounds that the Examiner has not met the prima facia case for 1) establishing a serious burden, 2) showing and giving a rational for a combination sub-combination restriction, and 3) showing and giving an example for a product and a process of using the product restriction. The Applicants detailed explanation is given in the Applicants' Office Action Response mailed on September 2, 2005 and is herein incorporated by reference.

Next, the Applicants have amended claim 16 to include the feature of a first embedded test circuit comprising a first ring oscillator coupled to a first test load, the first test load comprising a programmable interconnect structure formed in the first interconnect layer. As supported by paragraphs [0010], [0025], [0033], [0035], and [0038] of the specification, the interconnect structure formed in the first interconnect layer is programmable to different interconnect layouts, for example, see paragraph [0038]. Thus a FPGA or any IC comprising programmable interconnects can have different interconnect layouts on one or more interconnect layers.

Corr as illustrated by Fig. 6 [col. 7, lines 57-61] has hardwired, non-programmable interconnect layouts. Corr neither discloses nor suggests a programmable interconnect structure as required by claim 16 and hence for at least this reason alone claim 16 should be allowable.

Claims 17-20 and 23-25 being dependent upon claim 16 should be allowable for at least the reasons claim 16 is allowable.

In addition in claim 20 the IC comprises a field programmable gate array (FPGA), and wherein the FPGA is configured as a measurement circuit for reading a first output signal from the first embedded test circuit and a second output signal from the second embedded test circuit. As supported by paragraph [0003] of the

specification, and FPGA includes multiple configurable logic blocks connected via a programmable interconnect matrix. Corr neither disclose nor suggests analyzer 90 of Fig. 8 includes multiple configurable logic blocks connected via a programmable interconnect matrix. Thus for this reason alone claim 20 should be allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on February 28, 2006.

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